ALLOWANCE

1. Claims 1-5, 8, 11, 15, 18-19, 22, 25, 33, 36, 39-42 have been presented for examination. The Request for Continued Examination submitted 03/30/09 has been acknowledged. Claims 1-5, 8, 11, 15, 18-19, 22, 25, 33, 36, 39-42 are allowed over the prior art of record.

Response to Amendment

2. The 35 U.S.C 112, 2nd rejections have been withdrawn. The rejections of claims 34-35 have been withdrawn due to the canceled claims. The rejection of claim 40 has been withdrawn due to the amended claim.

3. The following is an examiner's statement of reasons for allowance:

Applicants disclose a system for evaluating simulators using a circuit design comprising: a processor; a reference simulator configured to generate golden data; a test simulator configured to generate test data; and a comparator to select test data and generate a comparison result by comparing a portion of the golden data to the portion of the test data wherein the comparison result is used to debug the test simulator by correcting and displaying an error detected in the comparison result. This has been disclosed in the prior art of record.

The prior art of record does not disclose the system wherein the reference simulator executes a first simulation image wherein the image is compiled from a first implementation of the circuit design, the test simulator executes a second simulation image which is compiled from a second implementation of the circuit design, *wherein the comparator uses a mapping rule of a plurality of mapping rules to identify a portion of the golden data associated with the portion of the test day, wherein the plurality of mapping rules map an internal hierarchy of the first implementation to an internal hierarchy of the second implementation, and the comparison result is generated by comparing the portions of the golden and test*

data before the execution of the second simulation image on the test simulator has completed, and wherein the reference simulator executes the first simulation image in lockstep with execution of the second simulation image.

U.S. Patent No. 6,141,630, McNamara: Discloses a system of ; a reference simulator configured to generate golden data by executing a first simulation image using the processor, wherein the first simulation image is complied from a first implementation of the circuit design **(column 5, lines 32-45)**; a test simulator **(column 3, lines 34-37 and Figure 1, testbench 108)** configured to generate test data by executing a second simulation image, wherein the second simulation image is compiled from a second implementation of the circuit design **(column 4, line 66 – column 5, line 4)**; and a comparator configured to select a portion of the test data **(column 4, lines 46-57 and column 5, 38-57)**, use a mapping rule of a plurality of mapping rules to identify a portion of the golden data associated with the portion of the test data, and generate a comparison result by comparing the portion of the golden data to the portion of the test data before the execution of the second simulation image on the test simulator has completed **(column 7, lines 18-36)** wherein the comparison result is used to debug the circuit design by correcting and displaying an error detected in the comparison result **(column 7, lines 19-31)**. However, McNamara fails to disclose the plurality of mapping rules map an internal hierarchy of the first implementation of the simulation design to an internal hierarchy of the second implementation and wherein the comparison result debugs the test simulator by correcting and displaying and error detected in the comparison result.

U.S. Patent No. 6,182,258, Hollander: Discloses a system of generating test for a circuit design by mapping two implementations of a circuit design wherein the plurality of mapping rules map an internal hierarchy of the first implementation of the simulation design to an internal hierarchy of the second implementation **(column 12, lines 40-49)**. However, Hollander fails to disclose using the mapping rules for a comparator wherein the comparison result debugs the test simulator by correcting and displaying and error detected in the comparison result.

U.S. Patent No. 7,178,063, Smith: Discloses a system of creating test cases for regression testing of software or hardware verification **(column 2, lines 47-50, column 2, line 60 – column 3, line 10)**. However, Smith fails to disclose the plurality of mapping rules map an internal hierarchy of the first implementation of the circuit simulation design to an internal hierarchy of the second implementation and wherein the comparison result debugs the test simulator by correcting and displaying and error detected in the comparison result.

U.S. Patent No. 6,601,024, Chonnad et al.: Discloses a system of translating circuit designs between hardware design languages wherein the multiple descriptions are compared to rectify functional discrepancy between the two descriptions **(column 5, lines 1-17)**. However, Chonmad fails to disclose the plurality of mapping rules map an internal hierarchy of the first implementation of the circuit simulation design to an internal hierarchy of the second implementation and wherein the comparison result debugs the test simulator by correcting and displaying and error detected in the comparison result.

Likewise, claims 11 and 25 also include method steps or system components not discloses by the prior art for the same reasons as noted above and therefore render claims 11 and 25 non-obvious over the prior art of record.

The Examiner interprets a specific computer for performing evaluation of test simulator inherent to the method of claim 11 as the method steps of claim 11 recite "executing a first/second simulation image" and further supported in paragraph [0030] wherein the invention is implemented on a computer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

1. U.S. Patent No. 6,678,645 B1 issued to Rajsuman et al. on 01/13/04.
2. U.S. Patent No. 6,625,759 B1 issued to Petsinger et al. on 09/23/03.
3. U.S. Patent No. 7,139,936 B2 issued to Petsinger et al. on 11/21/06.
4. U.S. Patent No. 6,606,721 B1 issued to Gowin, Jr. et al. on 08/12/03.
5. U.S. Patent No. 5,928,334 issued to Mandyam et al. on 07/27/99.
6. U.S. Patent No. 5,920,490 issued to Peters on 07/06/99.
7. U.S. Patent Application Publication 2005/0120278 A1 published by Smith et al. on 06/02/05.
8. U.S. Patent No. 7,017,150 B2 issued to Lam et al. on 03/21/06.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suzanne Lo whose telephone number is (571)272-5876. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2297. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/
Supervisory Patent Examiner, Art Unit 2128

/SL/
06/04/09